What Is Claimed Is:

1. A semiconductor device comprising:

a base substrate on one surface of which wiring patterns are formed;

a plurality of insulating layers located on and above said surface thereof;

conductor layers having wiring patterns formed therein and located on the insulating layers; and

semiconductor elements imbedded and mounted inside the insulating layers; wherein:

said wiring patterns are mutually electrically connected, passing through said insulating layers; and

said semiconductor elements are electrically connected to said wiring patterns.

2. The semiconductor device according to claim 1, wherein one or more semiconductor elements are imbedded and mounted inside each of said plurality of insulating layers.

3. The semiconductor device according to claim 1, wherein two or more semiconductor elements, respectively, are imbedded and mounted inside each of said plurality of insulating layers.

4. The semiconductor device according to claim 1, wherein thickness of said semiconductor elements is 50 μm or less.

5. The semiconductor device according to claim 1, wherein said semiconductor elements and wiring patterns corresponding thereto are electrically connected by flip chip mounting.

6. The semiconductor device according to claim 1, wherein said semiconductor elements and wiring patterns corresponding thereto are electrically connected via an anisotropically conductive film.

7. A semiconductor device manufacturing method comprising:

a first step for forming a wiring pattern on one surface of an insulative base substrate;

a second step for mounting a requisite number of semiconductor elements on said wiring pattern;

a third step for forming an insulating layer on said base substrate and said wiring pattern so as to cover said semiconductor elements;

a fourth step for forming via holes in said insulating layer so as to reach to said wiring pattern on said base substrate;

a fifth step for forming a conductor layer having a wiring pattern, on said insulating layer, inclusive of inner walls of said via holes;

a sixth step for repeating steps similar to said

second to fifth steps until a requisite number of wiring pattern layers is formed, and finally forming an insulating layer at the uppermost layer; and

a seventh step for forming, on other surface of said base substrate, external connection terminals which are electrically connected with said wiring patterns on said base substrate, passing through said base substrate.

8. The semiconductor device manufacturing method according to claim 7, wherein said seventh step comprises a step for effecting division so that one or more semiconductor elements are comprised inside each insulating layer, respectively.

9. The semiconductor device manufacturing method according to claim 7, wherein said seventh step comprises a step for effecting division so that two or more semiconductor elements are comprised inside each insulating layer, respectively.

10. The semiconductor device manufacturing method according to claim 7, wherein said via holes are formed by a laser beam machining in said fourth step.

11. The semiconductor device manufacturing method according to claim 7, wherein a photosensitive resin is used for material of said insulating layer in said third step,

and said via holes are formed by photolithography in said fourth step.

12. The semiconductor device manufacturing method according to claim 7, wherein, in said second step, said semiconductor elements and said wiring patterns corresponding thereto are electrically connected by flip chip mounting.

13. The semiconductor device manufacturing method according to claim 7, wherein, in said second step, said semiconductor elements and said wiring patterns corresponding thereto are electrically connected using an anisotropically conductive film.